

## REMARKS

This Amendment responds to the Office Action dated March 17, 2005 in which the Examiner rejected claims 1-9 under 35 U.S.C. §102(b).

As indicated above, claims 2 and 4 have been amended into independent form and the dependent claims 6-9 have been amended accordingly. New claims 10-13 correspond to claims 6-9 rewritten to depend from independent claim 4. The amendment is unrelated to a statutory requirement for patentability and does not change the literal scope of the claims.

Claims 2 and 4 claim a semiconductor storage device comprising a nonvolatile memory to which data is written in a sector unit, and a data rewriting unit rewriting data in the nonvolatile memory. Each sector in the nonvolatile memory includes: a data area into which data is stored; and a refresh mark into which information indicative of whether refresh has been performed or not is stored. The data rewriting unit includes a refresh execution unit referring to the refresh mark and whether the sector is refreshed or not, thereby executing the refresh. The data rewriting unit further includes a refresh zone detection unit dividing a block of the nonvolatile memory into refresh zone units for executing refresh and detecting the refresh zone including a sector of a writing target. The refresh execution unit refreshes the sector included in the refresh zone detected by the refresh zone detection unit every time data is written to a sector (for a predetermined number of times).

Through the structure of the claimed invention having a refresh execution unit refresh a sector every time data is written to a sector (for a predetermined number of times) as claimed in claims 2 and 4, the claimed invention provides a semiconductor

storage device which eliminates the need for a refresh counter and prevents the concentration of erasing/writing. The prior art does not show, teach or suggest the invention as claimed in claims 2 and 4.

Claims 1-9 were rejected under 35 U.S.C. §102(b) as being anticipated by So *et al* (U.S. Patent No. 6,151,246).

So *et al* appears to disclose a typical flash memory architecture which erases a sector as a unit and does not provide a mechanism for erasing or reducing the threshold voltage of individual memory cells. In such flash architectures, a sector containing a data error can be marked as requiring a refresh. Special memory cells in the array or a separate register can be used to identify the data sectors marked for a refresh. FIG. 6 illustrates a system 600 capable of performing scheduled or delayed refreshes of sectors. In system 600, an error detection circuit 655 detects data errors in data that a read circuit 650 reads from memory array 140. Error detection can occur as described above when a read circuit 650 reads a memory cell having a threshold voltage in a forbidden zone or as described below when a data value read is inconsistent with an error detection and correction code. When an error is detected, error detection circuit 655 marks the sector as requiring a refresh, for example by directing read/write control 670 to write a flag value in overhead memory cells in the sector containing the data error or write a sector number in a register in a refresh control 620. The refresh for a data sector marked as containing a data error need not be immediate. Instead refresh control 620 can wait for a period of inactivity of memory 600 before initiating a refresh operation on the marked sector. Alternatively, if the flag is stored in non-volatile memory, the refresh operation can occur during a start up procedure in which refresh control 620 checks for sectors

requiring a refresh operation. (Col. 8, line 45 through Col. 9, line 5) To determine when a differential sector should store the corrected values after a refresh, overhead memory cells in each sector can hold an erase count indicating the number of write/erase cycles for the sector and/or a refresh time indicating when the sector was last refreshed. Each erase cycle reads the erase count from a sector, erases the sector, and stores an incremented erase count in the overhead memory cells. Each refresh operation updates the refresh time in the sector. A sector can be declared invalid or defective during a refresh operation when the erase count is too high or when the last refresh time indicates a very short interval since the last refresh operation. The erase count is too high, for example, when the erase count exceeds a limit predetermined for the memory or determined relative to the erase counts in other sectors. When the erase count is too high or the last refresh was too recent, a refresh operation uses a spare sector in place of the invalid sector. (Col. 9, line 54 through col. 10, line 4)

Thus, *So et al* merely discloses refresh for a data sector, marked as containing a data error, can wait for a period of inactivity and if a flag is stored, the refresh operation can occur during a start up procedure (Col. 8, line 65 through col. 9, line 5). Thus nothing in *So et al* shows, teaches or suggests a refresh execution unit which refreshes a sector every time data is written to a sector (for a predetermined number of times) as claimed in claims 2 and 4. Rather, *So et al* teaches away from the claimed invention since the refresh can wait for a period of inactivity or can occur during a start up procedure.

Since nothing in *So et al* shows, teaches or suggests a refresh execution unit which refreshes a sector every time data is written to a sector (for a predetermined

number of times) as claimed in claims 2 and 4, applicant respectfully requests the Examiner withdraws the rejection to claims 2 and 4 under 35 U.S.C. §102(b).

Claims 3 and 5-13 depend from claims 2 and 4 and recite additional features. Applicant respectfully submits that claims 3 and 5-13 would not have been anticipated by *So et al* within the meaning of 35 U.S.C. §102(b) at least for the reasons as set forth above. Therefore, applicant respectfully requests the Examiner withdraws the rejection to the claims under 35 U.S.C. §102(b).

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested. Should the Examiner find that the application is not now in condition for allowance, applicant respectfully requests the Examiner enters this Amendment for purposes of appeal.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

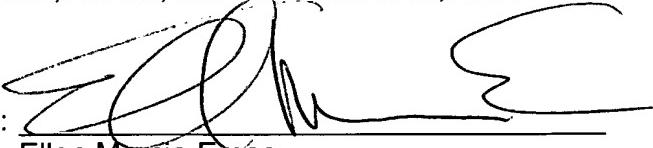
In the event that this paper is not timely filed within the currently set shortened statutory period, applicant respectfully petitions for an appropriate extension of time.

The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge  
our Deposit Account No. 02-4800.

Respectfully submitted,

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